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10/721,474	11/25/2003	Chimsong Sul	10030034-1	6056

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EXAMINER	
TRIMMINGS, JOHN P	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 03/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/721,474	SUL ET AL.	
	Examiner	Art Unit	
	John P. Trimmings	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☒ Claim(s) *1,13,14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-23 are presented for examination.

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference characters not mentioned in the description:

FIG.8 Compactor 39.

FIG.11 OFR Cell 46.

FIG.11 "XOR" 49.

2. The drawings are objected to under 37 CFR 1.83(a). The drawings of Figures 4 and 12 must show every feature of the invention specified in the claims. Therefore the features, wherein the device under test takes test address and control signals directly from the tester (Claim 13), and also wherein the device under test takes address and control signals directly from the test circuit (Claim 14) must be shown or the features canceled from the claims. No new matter should be entered.

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore the feature, wherein "the test channel inputs and configuration inputs of the test circuit are coupled to pins of the

[DUT]" (Claim 11) must be shown or the features canceled from the claims. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The disclosure is objected to because of the following informalities:

In regard to page 5, paragraph [20], last sentence, the examiner is not sure what the applicant is stating. The examiner believes that the applicant is saying that each scan chain contains a unique pattern defined by the corresponding bit of the n bits of the DE I/O signal. If the examiner's perception is correct, then the applicant is requested to reword the sentence.

Page 8 line 23 refers to "an exclusive OR or XOR operation", as if they were each mutually exclusive. In the interest of clarity, the examiner requests that the line be reworded to recite, "... such as an exclusive OR (XOR) operation, ...".

Page 9 line 19 should recite, "compactor 39", instead of "compactor 9".

Page 9 line 28 should recite, "Figure 9", instead of "Figure 8a".

Page 10 line 30 and page 11 line 2 each cite "OUT-FO", which is not in the drawing.

Page 11 line 5 cites "test system 1000" which is not in the drawing.

Appropriate correction is required.

Claim Objections

5. Claim 1 is objected to because of the following informalities: The preamble of the claim is not clear. The examiner requests that line 1 be amended to recite,

"1. A test circuit including:

at least one test channel input ...".

The examiner also requests that the applicant arrange the balance of the claim with proper punctuation and indentations so that one will be able to recognize the separate components of the test circuit.

6. Claim 13 is objected to because of the following informalities: The examiner requests that the applicant arrange the claim with proper punctuation and indentations so that one will be able to recognize the separate components of the test system.

7. Claim 14 is objected to because of the following informalities: The examiner requests that the applicant arrange the claim with proper punctuation and indentations so that one will be able to recognize the separate components of the test system.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 13 and 14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim contains subject matter that was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The claim refers to address and control signals coupled to pins of the DUT, and transferring data to the DUT for executing a test, all being a part of the test system of Claim 6. But the applicant has not disclosed such a test configuration, or the conditions required by one of ordinary skill to execute the test, and so the examiner has determined that the claim has not been enabled in the Specification.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 3, 9 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim limits operation of the test circuit to be either scan test or functional test mode, "responsive to the configuration signals". The configuration signals (Claims 1 and 6) control decoding algorithms of the test circuit. But scan and functional mode testing is controlled not by configuration signals, but by the configuration of the test circuit in FPGA logic, which is a completely different concept (see the applicant's recital of scan and functional test modes in paragraphs [26] and [27]). Therefore, the examiner is unsure of the meaning of "the configuration signals" in Claim 1, and so the claim is indefinite.

10. Claim 13 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The 3rd line of the claim, "... wherein the develops signals ..." is indefinite because the examiner is unsure of the subject matter of this phrase.

11. Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Line 5 of the claim recites, "... and [the tester] applies the decoded test data [N] on the test channel inputs ...". This limitation states that the output of the TMU (decoded test data) is applied back to the input of the TMU (test channel inputs of Claim 6). Such a limitation is not disclosed and is furthermore

indefinite. Because the examiner is not sure of what the applicant intends to claim, the examiner has determined therefore that the claim is indefinite.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. Claims 1, 3-6, 8-12 and 16-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Wang et al. (herein Wang), U.S. Patent Application No. 2003/0154433. As per Claim 1:

Wang teaches a test circuit including at least one test channel input (for example, see FIG.7 701), each test channel input (FIG.7 728, 729) being adapted to receive respective encoded test channel data (see discussion in paragraph [0007] and FIG. 2 215) and the test circuit (FIG.7) including configuration inputs (FIG.7 726, 727) adapted to receive configuration signals (see paragraph [0069] discussion on virtual scan inputs) and further including a plurality of decoded outputs (FIG.7 734-743), the test circuit being programmable responsive to the configuration signals to execute a desired decoding algorithm (paragraph [0069]), and being operable to apply the decoding algorithm to the encoded test channel data from each test channel input (FIG.7 702 with

705) and to develop decoded test data (FIG.7 734-743), the decoded test data including N bits(in this case 8 excluding copies of the inputs 726, 727) and the encoded test channel data including M bits (in this case 2), where N is greater than M (8>2), and the test circuit applying the decoded test data bits on the decoded outputs (outputs of FIG.7 701).

As per Claim 3:

Wang further teaches the test circuit of claim 1 wherein the test circuit operates in a scan test mode (FIG.12 scan mode in 1202 concurrent with functional inputs) and a functional test mode (FIG.12 1227, 1227 concurrent with scan input TDI) responsive to the configuration signals (decoded within the scan cells 1202), and wherein the test circuit executes different decoding algorithms (for example under control of 1228) during the scan and functional test modes (which run concurrently).

As per Claim 4:

Wang further teaches the test circuit of claim 3 wherein the test circuit couples each test channel input (FIG.12 1226, 1227) to a plurality of decoded outputs (FIG.12 1215-1223) to define the decoding algorithm executed during the scan test mode (under control of 1228).

As per Claim 5:

Wang further teaches the test circuit of claim 1 wherein M<N<2^(M+1). The examiner has substituted the circuit of FIG.5A, where N=8 and M=3, therefore 3<8<16.

As per Claim 6:

Wang teaches a test system (FIG.2 201), comprising: a tester (FIG.2 202) operable to provide encoded test channel data on at least one test channel output (see discussion in paragraph [0007] and FIG. 2 215); a test circuit (FIG.2 207 or FIG.7) including at least one test channel input (FIG.7 728, 729), each test channel input being coupled to a corresponding test channel output (FIG.2 215) to receive encoded test channel data (paragraph [0007]) and the test circuit including configuration inputs adapted to receive configuration signals (FIG.7 726, 727) and further including a plurality of decoded outputs (FIG.7 730-733), the test circuit being programmable responsive to the configuration signals to execute a desired decoding algorithm (paragraphs [0066] and [0067]), and being operable to apply the decoding algorithm to the encoded test channel data from each test channel input and to develop decoded test data (FIG.7 734-743), the decoded test data including N bits (10) and the encoded test channel data including M bits (2), where N (10) is greater than M (2), and the test circuit applying the decoded test data bits on the decoded outputs (FIG.7 702 outputs 734-743); and a device under test (FIG.7 724) including circuitry (see FIG.2 209, 212) and including a plurality of pins coupled to the circuitry (FIG.2 209 inputs and outputs), and at least some of the pins being coupled to the decoded outputs of the test circuit (see FIG.7 734-743) to receive decoded test data bits (paragraphs [0066] and [0067]).

As per Claim 8:

Wang further teaches the test system of claim 6 wherein the tester applies the configuration signals to the test circuit. The "Virtual Scan Inputs" of FIG.7, 726 and 727, relate to the FIG.2 signal 215, which is outputted from the ATE 202.

As per Claim 9:

Wang further teaches the test system of claim 6 wherein the test circuit operates in a scan test mode (FIG.12 scan mode in 1202 concurrent with functional inputs) and a functional test mode (FIG.12 1227, 1227 concurrent with scan input TDI) responsive to the configuration signals (decoded within the scan cells 1202), and wherein the test circuit executes different decoding algorithms (for example under control of 1228) during the scan and functional test modes (which run concurrently).

As per Claim 10:

Wang further teaches the test system of claim 9 wherein the test circuit couples each test channel input (FIG.12 1226, 1227) to a plurality of decoded outputs (FIG.12 1215-1223) to define the decoding algorithm executed during the scan test mode (under control of 1228).

As per Claim 11:

Wang further teaches the test system of claim 6 wherein the test circuit is physically formed within the device under test, and wherein the test channel inputs and configuration inputs of the test circuit are coupled to pins of the device under test (see paragraph [0010]).

As per Claim 12:

Wang further teaches the test system of claim 11 wherein the test circuit operates in a scan test mode (FIG.12 scan mode in 1202 concurrent with functional inputs) and a functional test mode (FIG.12 1227, 1227 concurrent with scan input TDI) responsive to the configuration signals (decoded within the scan cells 1202), and

wherein the test circuit executes different decoding algorithms (for example under control of 1228) during the scan and functional test modes (which run concurrently).

As per Claim 16:

Wang further teaches a method of testing a device under test (see Title) having a plurality of pins M (FIG.5A Y0-Y7) with a tester having a plurality of test channels N (FIGl.5A X1-X3), where N (3) is less than M (8), the method comprising: coupling a plurality of pins on the device under test to the test channels on the tester (paragraph [0010]); transferring test data into the device under test over the test channels coupled to the pins on the device under test (paragraph [0011]); testing the device under test using the transferred test data (paragraph [0055]); and providing from the device under test an indication of the results of the test (paragraph [0049]).

As per Claim 17:

Wang further teaches the method of claim 16 wherein testing the device under test using the transferred test data comprises executing a scan test in the device under test (paragraph [0047]).

As per Claim 18:

Wang further teaches the method of claim 16 wherein providing from the device under test an indication of the results of the test comprises compacting internal test data within the device under test to generate a signature and providing the signature from the device under test (paragraph [0049]).

As per Claim 19:

Wang teaches a method of testing a device under test having a plurality of external pins M (FIG.5A Y0-Y7) with a tester having a plurality of test channels N (FIG.5A X0-X2), where N (3) is less than M (8), the method comprising: applying test data on each of the test channels (FIG.5A X0-X2), the test data on each channel including X bits (assume 1 bit); generating from the test data applied on each test channel expanded test data having Y bits (in the case of signal X1, the signal expands to Y2, Y3, Y4), where Y (3) is greater than X (1); applying the respective bits of expanded test data on Y external pins of the device under test (FIG.5A 508); testing the device under test using the expanded test data applied on the pins (paragraph [0055]); and providing from the device under test an indication of the results of the test (paragraph [0049])..

As per Claim 20:

Wang further teaches the method of claim 19 wherein generating from the test data applied on each test channel expanded test data and applying the respective bits of the expanded test data comprise: during a scan test mode of operation, generating expanded test data having a first group of Y bits (using X1; FIG.5A Y2, Y3, Y4); applying the respective bits of expanded test data in the first group on a first group of Y external pins of the device under test (Y2, Y3, Y4); during a functional test mode of operation, generating expanded test data having a second group of Y bits (using X2; FIG.5A Y4, Y6, Y7); applying the respective bits of expanded test data in the second group on a second group of Y (FIG.5A Y4, Y6, Y7) external pins of the device under test.

As per Claim 21:

Wang further teaches the method of claim 20 wherein the first group of Y bits (Y2, Y3, Y4) is different than the second group of Y bits (Y4, Y6, Y7) and wherein the second group of Y external pins is the same (3 pins each) as the first group of Y external pins.

As per Claim 22:

Wang further teaches the method of claim 19 wherein testing the device under test using the expanded test data applied on the pins comprises executing a scan test in the device under test (paragraph [0047]).

As per Claim 23:

Wang further teaches the method of claim 19 wherein providing from the device under test an indication of the results of the test comprises compacting internal test data within the device under test to generate a signature and providing the signature from the device under test (paragraph [0049]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 2, 7 and15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (herein Wang), U.S. Patent Application No. 2003/0154433, in view of Mielke et al. (herein Mielke), U.S. Patent No. 6195772. The claims each limit the test circuit to being an FPGA. FPGA's are also referred to as PLA devices (see Google definition of "Programmable Logic Device"), and so where Wang fails to further disclose the test circuit to be an FPGA, Mielke does, in FIG.1 Pin Channel Board 50, where test interfacing units 52a – 52c are "configured" to interface the DUT with the tester controller (FIG.3 210). The interfacing of DUT signals is utilized by configuring the PLA units to adapt to test data/vectors and control inputs to a DUT (column 1 lines 60-67 and column 2 lines 23-33) automatically, without intervention. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to include the PLA devices of Mielke with the tester interface of Wang in order to quickly adapt vector and data inputs to the DUT without any intervention.

14. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (herein Wang), U.S. Patent Application No. 2003/0154433, in view of Correale, Jr. et al. (herein Correale), U.S. Patent No. 6001662.

As per Claim 13:

Wang fails to further disclose the test system of claim 6 wherein the tester further includes test data inputs and address and control outputs coupled to pins on the device under test, and wherein the (?) develops signals on the address and control outputs to transfer decoded test data into the device under test via the test circuit, and wherein the

device under test provides results test data on the test data inputs and the tester operates to analyze the test data to detect defects in the device under test. Claim 13 is rejected under 35 USC 112 first and second paragraphs (see above). In view of the rejections above, the examiner has included a 2nd referenced ABIST (Correale, FIG.6 120) which takes in address (FIG.6 146) and control (FIG.6 144) signals from the tester to control addressing and testing of the DUT (see FIG.5) and analysis of the testing to detect defects (see FIG.5). And column 2 lines 30-36 cite an advantage of Correale being a system to test various sized memory arrays using a single ABIST design. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to include a BIST (as applied to the claim) with the capability to test any sized memory in a system of Wang when needing to adapt to various memory sizes under production.

As per Claim 14:

Wang fails to further disclose the test system 6 wherein the test circuit and device under test collectively form a test bench, and wherein the tester provides an initialization signal to the test circuit on a test channel output and wherein, responsive to the initialization signal, the test circuit generates the configuration signals to execute the desired decoding algorithm and applies the decoded test data on the test channel inputs, the test circuit being further operable to apply address and control signals along with the decode test data to the device under test, wherein the device under test executes a test responsive to the address and control signals and decoded test data and applies a signature signal to the test circuit indicating the results of the test, and

wherein the test circuit, responsive to the signature, processes the signature and applies a status signal to the tester indicating the results of the test. Claim 14 is rejected under 35 USC 112 first and second paragraphs (see above). In view of the rejections above, the examiner has included a 2nd referenced ABIST (Correale, FIG.6 120) which takes in address (FIG.6 146) and control (FIG.6 144) signals from the tester to control addressing and testing of the DUT (see FIG.5) and analysis of the testing to detect defects (see FIG.5). And column 2 lines 30-36 cite an advantage of Correale being a system to test various sized memory arrays using a single ABIST design. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to include a BIST (as applied to the claim) with the capability to test any sized memory in a system of Wang when needing to adapt to various memory sizes under production.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2138

jpt

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